We claim:

1. An integrated circuit, comprising:

a data processing unit;

a buffer memory having registers for storing data for said data processing unit, said buffer memory connected to said data processing unit; and

a setting memory connected to said buffer memory, said setting memory at least one of being written to and being read from through said buffer memory.

2. The integrated circuit according to claim 1, including circuit elements, said setting memory activating said circuit elements.

3. The integrated circuit according to claim 2, including a memory having memory areas, said circuit elements being memory elements used to replace at least one of said memory areas.

4. The integrated circuit according to claim 1, wherein said processing unit has an arithmetic logic unit.

5. The integrated circuit according to claim 4, wherein

a register of said registers processes data; and

another register of said registers processes coded instructions for said arithmetic logic unit.

6. The integrated circuit according to claim 5, wherein said buffer memory is two buffer memories each containing data to be processed.

7. The integrated circuit according to claim 1, wherein said buffer memory is a latch.

8. The integrated circuit according to claim 1, wherein said buffer memory has a shift register.

9. The integrated circuit according to claim 8, wherein said shift register has at least one switch subdividing said shift register into registers for said processing unit.

10. The integrated circuit according to claim 1, wherein said processing unit serially writes to and reads from each of said registers.

11. The integrated circuit according to claim 1, wherein said setting memory has electrical fuses.

12. A method for determining setting data for a setting memory from address data, stored in a register, of memory areas of a memory that have been identified as defective depending on instruction data stored in a register, which comprises:

providing an integrated circuit having:

a data processing unit;

a buffer memory having register; and

a setting memory;

storing data for the data processing unit in registers of the buffer memory;

connecting the buffer memory to the data processing unit;

connecting the setting memory to the buffer memory; and

at least one of the group selected from writing to and reading from the setting memory through the buffer memory.

13. The method according to claim 12, which further comprises activating circuit elements with the setting memory.

14. The method according to claim 13, wherein the circuit elements are memory elements of a memory and which further comprises replacing at least one of the memory areas with the memory elements.

15. The method according to claim 12, wherein the processing unit has an arithmetic logic unit.

16. The method according to claim 15, which further comprises:

processing data with a register; and

processing coded instructions for the arithmetic logic unit with another register.

17. The method according to claim 16, wherein the buffer memory is two buffer memories each containing data to be processed.

18. The method according to claim 12, wherein the buffer memory is a latch.

19. The method according to claim 12, wherein said buffer memory has a shift register.

20. The method according to claim 19, which further comprises subdividing the shift register into registers for the processing unit with at least one switch of the shift register.

21. The method according to claim 12, which further comprises serially writing to and reading from each of the registers with the processing unit.

22. The method according to claim 12, wherein the setting memory has electrical fuses.